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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,630	12/03/2001	John A. Morrison	100111514-1	7448

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EXAMINER

YIGDALL, MICHAEL J

ART UNIT

PAPER NUMBER

2122

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/998,630

Applicant(s)

MORRISON ET AL.

Examiner

Michael J. Yigdal

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

1. Claims 1-22 are pending and have been examined. The priority date considered for the application is December 3, 2001.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6, 9-14 and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pub. No. 2002/0091807 to Goodman (hereinafter "Goodman").

With respect to claim 1, Goodman discloses a system for loading firmware in a high availability system (see the abstract) comprising:

(a) a high speed interconnect (see communication interface or interconnect 42 in FIG. 1, and page 2, first column, lines 10-17);

(b) a mismatched cell coupled to the high speed interconnect and comprising errored firmware (see page 2, second column, lines 20-28 and 35-37, which shows a node or cell, i.e. a mismatched cell, coupled to the interconnect having incompatible or errored firmware), the mismatched cell configured to enable the high speed interconnect (see page 3, first column, lines 9-12, which shows that the mismatched cells enable communications over the interconnect);

(c) an update cell coupled to the high speed interconnect and comprising update firmware (see page 2, second column, lines 29-35, which shows a node or cell, i.e. an update cell, coupled to the interconnect having updated firmware), the update cell configured to load the update firmware to the mismatched cell via the high speed interconnect at a first rendezvous (see page 3, second column, lines 8-20, which shows that the update cell loads the updated firmware to the mismatched cells over the interconnect); and

(d) a boot block configured to reset the mismatched cell and the update cell through to the first rendezvous (see page 3, second column, lines 20-29, which shows a boot block to reset the nodes or cells).

With respect to claim 2, Goodman further discloses the limitation wherein the system further comprises correction firmware configured to determine that processor dependent code is not resident on the high availability system and, in response, to boot the boot block (see page 2, second column, lines 41-54, which shows correction firmware to check and boot the nodes, and page 3, first column, lines 36-42, which shows determining that the correct code is not resident; see also page 2, second column, lines 12-15, which shows that the firmware comprises code for a specific node, i.e. processor dependent code).

With respect to claim 3, Goodman further discloses the limitation wherein the system further comprises processor dependent code and correction firmware, the correction firmware configured to determine that a checksum for the processor dependent code is not correct and, in response, to boot the boot block (see page 2, second column, lines 41-54, which shows correction firmware to check and boot the nodes, and page 3, first column, lines 36-42, which

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shows determining that the signature or checksum for the code is not correct; see also page 2, second column, lines 12-15, which shows that the firmware comprises code for a specific node, i.e. processor dependent code).

With respect to claim 4, Goodman further discloses the limitation wherein the update cell further is configured to determine at the first rendezvous that the update firmware is a desired version of firmware and, thereafter, to load the update firmware to the mismatched cell via the high speed interconnect (see page 3, second column, lines 8-20, which shows loading the desired version of firmware from the update cell to the mismatched cells over the interconnect).

With respect to claim 5, Goodman further discloses a second mismatched cell comprising second errored firmware (see page 2, second column, lines 20-28 and 35-37, which shows a node or cell, i.e. a second mismatched cell, coupled to the interconnect having incompatible or errored firmware), the second mismatched cell configured to enable the high speed interconnect (see page 3, first column, lines 9-12, which shows that the mismatched cells enable communications over the interconnect);

wherein the boot block further is configured to reset the second mismatched cell only through to the first rendezvous (see page 3, second column, lines 20-29, which shows that the boot block resets the nodes or cells); and

wherein the update cell further is configured to load the update firmware to the second mismatched cell via the high speed interconnect (see page 3, second column, lines 8-20, which shows that the update cell loads the updated firmware to the mismatched cells over the interconnect).

With respect to claim 6, Goodman further discloses the limitation wherein the errored firmware comprises at least one member of a group consisting of firmware that is not a latest version of firmware and corrupt firmware (see page 3, first column, lines 36-42, which shows that the errored firmware comprises firmware that is not the latest version of firmware).

With respect to claim 9, Goodman discloses a method for loading firmware in a high availability system (see the abstract) comprising a high speed interconnect (see communication interface or interconnect 42 in FIG. 1, and page 2, first column, lines 10-17) and at least a mismatched cell and an update cell, the mismatched cell coupled to the high speed interconnect and comprising errored firmware such that the high speed interconnect is not enabled for the mismatched cell (see page 2, second column, lines 20-28 and 35-37, which shows a node or cell, i.e. a mismatched cell, coupled to the interconnect having incompatible or errored firmware, and lines 29-35, which shows that the mismatched cell may be disabled, i.e. not enabled for the interconnect), the update cell coupled to the high speed interconnect and comprising update firmware (see page 2, second column, lines 29-35, which shows a node or cell, i.e. an update cell, coupled to the interconnect having updated firmware), the method comprising:

(a) using a boot block to reset the mismatched cell and the update cell to a first rendezvous (see page 3, second column, lines 20-29, which shows a boot block resetting the nodes or cells);

(b) enabling the high speed interconnect from the mismatched cell at the first rendezvous (see page 3, first column, lines 9-12, which shows the mismatched cells enabling communications over the interconnect); and

(c) loading the update firmware from the update cell to the mismatched cell via the high speed interconnect (see page 3, second column, lines 8-20, which shows the update cell loading the updated firmware to the mismatched cells over the interconnect).

With respect to claim 10, the limitations recited in the claim are analogous to the limitations recited in claim 2 (see the reasoning applied to claim 2 above).

With respect to claim 11, the limitations recited in the claim are analogous to the limitations recited in claim 3 (see the reasoning applied to claim 3 above).

With respect to claim 12, the limitations recited in the claim are analogous to the limitations recited in claim 4 (see the reasoning applied to claim 4 above).

With respect to claim 13, the limitations recited in the claim are analogous to the limitations recited in claim 5 (see the reasoning applied to claim 5 above).

With respect to claim 14, the limitations recited in the claim are analogous to the limitations recited in claim 6 (see the reasoning applied to claim 6 above).

With respect to claim 17, Goodman discloses a method for loading firmware in a high availability system (see the abstract) comprising a manageability system (see page 2, first column, lines 41-47, which shows a system coupled to each node or cell for applying firmware updates, i.e. a manageability system), a high speed interconnect (see communication interface or interconnect 42 in FIG. 1, and page 2, first column, lines 10-17), and a plurality of cells, the plurality of cells each coupled to the manageability system and coupled to the high speed

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interconnect but not enabled for the high speed interconnect (see page 2, second column, lines 29-35, which shows a plurality of nodes or cells coupled to the interconnect that may be disabled, i.e. not enabled for the interconnect), the method comprising:

(a) loading a boot block via the manageability system to at least a first memory location of at least a first cell (see page 2, second column, lines 41-54, which shows loading a boot block to a node or cell, i.e. a first cell);

(b) loading update firmware via the manageability system to at least a second memory location of at least an update cell (see page 2, second column, lines 29-35, which shows loading updated firmware to a node or cell, i.e. an update cell);

(c) using the boot block of the first cell to reset the cells to a first rendezvous (see page 3, second column, lines 20-29, which shows the boot block resetting the nodes or cells);

(d) enabling the high speed interconnect for the cells at the first rendezvous (see page 3, first column, lines 9-12, which shows enabling communications over the interconnect); and

(e) loading the update firmware from the update cell to the other cells via the high speed interconnect (see page 3, second column, lines 8-20, which shows loading the updated firmware from the update cell to the other cells over the interconnect).

With respect to claim 18, Goodman further discloses loading the boot block to other first memory locations of a plurality of the cells via the manageability system (see page 2, second column, lines 41-54, which shows loading the boot block to the nodes or cells).

With respect to claim 19, Goodman further discloses:

(a) loading the boot block to other first memory locations of only other cells that do not have a desired version of firmware (see page 4, first column, lines 15-31, which shows loading the update routine, which includes the boot block, to nodes or cells that do not have a desired version of firmware); and

(b) loading the update firmware to other second memory locations of only other cells that do not have the desired version of firmware (see page 3, first column, line 65 to second column, line 6, which shows loading the code, i.e. the update firmware, to only the nodes or cells that do not have a desired version of firmware).

With respect to claim 20, Goodman further discloses the limitation wherein the loading the boot block to the first memory location comprises at least one member of a group comprising loading the boot block to a non-volatile memory location and loading the boot block to a firmware storage element location (see page 2, first column, lines 47-55, which shows non-volatile memory and a firmware storage element).

With respect to claim 21, Goodman further discloses the limitation wherein the loading the update firmware to the second memory location comprises at least one member of a group comprising loading the update firmware to a non-volatile memory location and loading the update firmware to a firmware storage element location (see page 2, first column, lines 47-55, which shows non-volatile memory and a firmware storage element).

With respect to claim 22, Goodman further discloses the limitation wherein the first cell is the update cell and the step of loading the update firmware via the manageability system to the second memory location of the update cell comprises loading the update firmware via the

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manageability system to the second memory location of the first cell (see page 2, second column, lines 29-35, which shows loading updated firmware to the first cell or update cell).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 7, 8, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodman, as applied to claims 1 and 9 above, respectively, in view of U.S. Pat. No. 6,334,177 to Baumgartner et al. (hereinafter "Baumgartner").

With respect to claim 7, although Goodman discloses a communication interface or interconnect used for both messages (see page 3, first column, lines 5-12) and firmware (see page 3, second column, lines 8-20), Goodman does not expressly disclose a separate manageability system interconnect.

However, Baumgartner discloses a non-uniform memory access system having a plurality of nodes or cells (see the title and abstract) connected by a high-speed interconnect (see interconnect 16 in FIG. 1, and column 3, lines 13-19), and a manageability system interconnect (see bus 12 in FIG. 1, and column 3, lines 2-9), over which commands are transmitted (see column 5, lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the firmware update features of Goodman within the architecture taught by Baumgartner, in order automatically maintain compatible firmware among nodes (see Goodman, page 1, second column, lines 19-29) in a multiprocessor system that further provides speed advantages and simplified programming (see Baumgartner, column 1, lines 41-48).

Therefore, Goodman in view of Baumgartner further discloses:

a manageability system interconnect (see Baumgartner, bus or interconnect 12 in FIG. 1, and column 5, lines 11-13, which shows receiving commands or messages, i.e. manageability system commands, over the interconnect);

wherein the mismatched cell is configured to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect and to enable the high speed interconnect (see Goodman, page 3, first column, lines 5-12, which shows the mismatched cells receiving a code signature, i.e. an update message, and enabling communications over the interconnect, i.e. with an acknowledgement); and

wherein the update cell further is configured to generate an update menu, to receive an update command generated via the update menu (see Goodman, page 3, first column, line 53 to second column, line 3, which shows checking the code signature of each node, i.e. generating an update menu, and selecting a node from the menu to provide the update, i.e. generating an update command), and, in response thereto, to transmit the update message to the mismatched cell and, after receiving the acknowledgment, to load the update firmware to the mismatched cell via the high speed interconnect (see Goodman, page 3, second column, lines 8-20, which shows the

update cell broadcasting or transmitting the firmware, i.e. an update message, to the mismatched cells and subsequently loading the firmware over the interconnect).

With respect to claim 8, although Goodman discloses a communication interface or interconnect used for both messages (see page 3, first column, lines 5-12) and firmware (see page 3, second column, lines 8-20), Goodman does not expressly disclose a separate manageability system interconnect.

However, Baumgartner discloses a non-uniform memory access system having a plurality of nodes or cells (see the title and abstract) connected by a high-speed interconnect (see interconnect 16 in FIG. 1, and column 3, lines 13-19), and a manageability system interconnect (see bus 12 in FIG. 1, and column 3, lines 2-9), over which commands are transmitted (see column 5, lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the firmware update features of Goodman within the architecture taught by Baumgartner, in order automatically maintain compatible firmware among nodes (see Goodman, page 1, second column, lines 19-29) in a multiprocessor system that further provides speed advantages and simplified programming (see Baumgartner, column 1, lines 41-48).

Therefore, Goodman in view of Baumgartner further discloses:

a manageability system interconnect (see Baumgartner, bus or interconnect 12 in FIG. 1, and column 5, lines 11-13, which shows receiving commands or messages, i.e. manageability system commands, over the interconnect);

wherein the mismatched cell further is configured to receive an update message via the manageability system interconnect and, in response thereto, to enable the high speed interconnect

(see Goodman, page 3, first column, lines 5-12, which shows the mismatched cells receiving a code signature, i.e. an update message, and enabling communications over the interconnect); and

wherein the update cell further is configured to transmit the update message to the mismatched cell and, thereafter, to automatically load the update firmware to the mismatched cell via the high speed interconnect (see Goodman, page 3, second column, lines 8-20, which shows the update cell broadcasting or transmitting the firmware, i.e. an update message, to the mismatched cells and subsequently loading the firmware over the interconnect).

With respect to claim 15, the limitations recited in the claim are analogous to the limitations recited in claim 7 (see the reasoning applied to claim 7 above).

With respect to claim 16, the limitations recited in the claim are analogous to the limitations recited in claim 8 (see the reasoning applied to claim 8 above).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. U.S. Pat. No. 6,055,632 to Deegan et al. discloses a method and apparatus for transferring firmware to a non-volatile memory of a programmable controller system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.


After October 25, 2004, the examiner can be reached at (571) 272-3707, and the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3694.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

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